Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.030”**

**.030”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: S = .0045” X .0055” G = .004” X .004”**

**Backside Potential: Drain**

**Mask Ref: VF21**

**APPROVED BY: DK DIE SIZE .030” X .030” DATE: 11/9/22**

**MFG: SUPERTEX THICKNESS .011” P/N: 2N6660**

**DG 10.1.2**

#### Rev B, 7/19/02